REMARKS

Reconsideration and allowance of this application, as amended, are respectfully requested. Claims 23-27 have been cancelled. Claims 1, 2, 4-17, 19-22 and 28-36 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the remarks presented herein.

As a preliminary matter, another Supplemental Application Data Sheet supplying the inventor's P.O. address is filed concurrently.

Rejection Under 35 U.S.C. § 102(e) - Massoudi

Claims 1 and 10 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Massoudi (U.S. Patent Number 6,363,511). The rejection is respectfully traversed.

Regarding independent claims 1 and 10, the claimed invention relates to a decoder comprising a storing part, a control part, a first RS core for calculating a first error location and a first error value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part.

Turning to the cited art, the disclosure of Massoudi does not anticipate the claimed invention. Massoudi describes a device for detecting and correcting errors in error correction coded data blocks read sequentially from a DVD medium. As shown in Figure 6, Massoudi's error detection and correction circuitry includes on-the-fly row correction circuitry 410, correction control circuitry 606, correction engine 608 and correction circuitry 602. However, Massoudi does not disclose a first RS core for calculating a first error location and a first error

value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part, as claimed. Massoudi's correction engine 608 uses syndromes, generated by the on-the-fly row correction circuitry 410 and column and EDC syndrome generator circuitry 412, to "generate an 'error value' and 'error location' for the row or column associated with the syndrome" (column 9, lines 43-46). The generated error value is then used by either the on-the-fly row correction circuitry 410 or the correction circuitry 602 to correct the errors (column 9, lines 46-49). The on-the-fly row correction circuitry 410 and the correction circuitry 602 do not calculate error location/values. Instead, only Massoudi's correction engine 608 calculates an error value and error location. On-the-fly correction circuitry 410 and correction circuitry 602 merely use the error location/values generated by the correction engine 608 (see column 9, lines 43-49). Applicant's claimed decoder comprises a first RS core as well as a second RS core, each calculating respective error location/values from data read from the storing part. Examiner has asserted that row syndromes are generated and row error correction is performed on-the-fly, and that "on the fly error correction for the Reed-Solomon encoded rows is performed separately from the error correction for the Reed-Solomon encoded column." Examiner also asserts that the decoding and correction of Reed-Solomon error correction codes inherently requires steps for determining the error value and location in order for a codeword to be corrected. These assertions are not supported by Massoudi.

There is no basis for this contention of inherency, because Massoudi explicitly discloses that all error location and error value calculations are performed only by the correction engine

608. The on-the-fly row correction circuitry 410, column and EDC syndrome generator circuitry 412 and row syndrome generator circuitry 604 only serve to provide syndromes to the correction engine 608 as a basis with which the correction engine 608 performs the error location and error value calculations. Furthermore, the on-the-fly row correction circuitry 410 (Examiner's interpretation of the first RS core)and correction circuitry 602 (Examiner's interpretation of the second RS core) use the error location and error value calculations received from the correction engine 608 to perform row and column corrections, however, neither the on-the-fly row correction circuitry 410 nor the correction circuitry 602 **calculate** error location or error values from the ECC block data stream. This element is explicitly recited in Applicant's claims. At least by virtue of the aforementioned differences, the invention defined by claims 1 and 10 is patentable over Massoudi. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) are respectfully requested.

Rejection Under 35 U.S.C. § 102(e) - Fujita et al.

Claims 15 and 16 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Fujita et al. (U.S. Patent Number 6,131,178; hereinafter "Fujita"). The rejection is respectfully traversed.

Regarding independent claim 15, the claimed invention relates to a decoding method comprising reading data to be decoded and an eraser flag, calculating an error location and an error value from the read data, correcting an error of the data according to the calculated error location and error value, and decoding the data. The calculation step comprises a first calculation step for calculating a first error location and a first error value from the read data, and

a second calculation step for calculating a second error location and a second error value from

the read data.

Turning to the cited art, the disclosure of Fujita does not anticipate the claimed invention.

Fujita describes an error correction apparatus for singly extended Reed-Solomon code or double

extended Reed-Solomon code. The Examiner cites to Figures 21 and 24 as teaching the claimed

invention, however, there is no showing or mention in Fujita of both a first calculation step for

calculating a first error location and a first error value from the read data, and a second

calculation step for calculating a second error location and a second error value from the read

data. Furthermore, the Examiner admits in paragraph 7 of the Office Action dated July 13, 2004,

that "Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders]." At least

by virtue of the aforementioned differences, the invention defined by claim 15 is patentable over

Fujita. Claim 16 is a dependent claim including all of the elements of independent claim 15,

which, as established above, is patentable over Fujita. Therefore, claim 16 is patentable over

Fujita for at least the aforementioned reasons as well as for its additionally recited features.

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) are respectfully

requested.

Rejection Under 35 U.S.C. § 103(a) - Massoudi in view of Fujita et al.

Claims 4-9, 11-14, 28 and 29 are rejected under 35 U.S.C. § 103(a) as allegedly being

unpatentable over Massoudi in view of Fujita. The rejection is respectfully traversed.

Referring to amended independent claims 1 and 10, the claimed decoder comprises a first

RS core as well as a second RS core, each calculating respective error location/values from data

read from the storing part. Neither Massoudi nor Fujita disclose both a first RS core for calculating a first error location and a first error value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part, as claimed. Instead, only Massoudi's correction engine 608 "generate[s] an 'error value' and 'error location' for the row or column associated with the syndrome" (column 9, lines 43-46). On-the-fly correction circuitry 410 and correction circuitry 602 solely use the error location/values generated by the correction engine 608 (see column 9, lines 43-49), and do not themselves generate any error value or error location.

Turning to Fujita, the Examiner has also previously admitted in the Office Action dated July 13, 2004, that "Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders]." Thus, Fujita also does not disclose both a first RS core and a second RS core, as claimed. At least by virtue of the aforementioned differences, the invention defined by independent claims 1 and 10 is patentable over Massoudi in view of Fujita. Claims {4-9} and {11-14, 28 and 29} are dependent claims including all of the elements of independent claims 1 and 10, respectively, which, as established above, is patentable over Massoudi in view of Fujita. Therefore, claims 4-9, 11-14, 28 and 29 are patentable over Massoudi in view of Fujita for at least the aforementioned reasons as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Rejection Under 35 U.S.C. § 103(a) - Fujita et al. in view of Massoudi

Claims 19-22 and 30 are rejected under 35 U.S.C. § 103(a) as allegedly being

unpatentable over Fujita in view of Massoudi. The rejection is respectfully traversed.

Regarding amended independent claim 15, the claimed decoder comprises both a first

calculation step for calculating a first error location and a first error value from the read data, and

a second calculation step for calculating a second error location and a second error value from

the read data. The Examiner admits in paragraph 7 of the Office Action dated July 13, 2004, that

"Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders]." Massoudi

also does not disclose both a first calculation step and a second calculation step to obtain error

locations and error values used to correct an error of the data which is then decoded, as

Applicant's claim recites. As described above, only Massoudi's correction engine 608

"generates an 'error value' and 'error location' for the row or column associated with the

syndrome" (column 9, lines 43-46). On-the-fly correction circuitry 410 and correction circuitry

602 solely use the error location/values generated by the correction engine 608 (see column 9,

lines 43-49), and do not themselves generate any error value or error location. Thus, Massoudi

only teaches a single calculation step/core, which is completely performed by the correction

engine 608. At least by virtue of the aforementioned differences, the invention defined by

independent claim 15 is patentable over Fujita in view of Massoudi. Claims 19-22 and 30 are

dependent claims including all of the limitations of independent claim 15, which, as established

above, is patentable over Fujita in view of Massoudi. Therefore, claims 19-22 and 30 are

patentable over Fujita in view of Massoudi for at least the aforementioned reasons as well as for

their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

With further regard to claim 19, neither Fujita nor Massoudi even mention a calculation step as Applicant claims, in which an eraser location polynomial calculation step calculates an eraser location polynomial from the read eraser flag, a first syndrome polynomial calculation step calculates a first syndrome polynomial from the read data, a first errata location polynomial calculation step calculates a first errata location polynomial from the calculated eraser location polynomial and the first syndrome polynomial, and outputs the first errata location polynomial and the delayed first syndrome polynomial, and a first error location/value calculation step calculates a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial. At least by virtue of this additional difference as well as the aforementioned differences, Applicant's claimed invention distinguishes over Fujita in view of Massoudi.

Allowable Claims 31-36

Regarding claims 31-36, claims 31-36 are allowable over the cited references based on at least their dependencies as well as for their additionally recited features. That is, the cited references do not teach or suggest a number "m" which may be appropriately determined according to a data representation method and which represents an amount of data, as recited in claims 31, 33 and 36. The cited references also fail to teach or suggest a parallel operation of a first RS core and a second RS core calculating error locations and error values from data, as recited in claims 32 and 34.

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AMENDMENT UNDER 37 C.F.R. § 1.116
U.S. Application No. 10/066,651
Attorney Docket No. Q64314

In view of the above, reconsideration and allowance of this application are now believed

to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

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